REMARKS/ARGUMENTS

Claims 1-16 and 18-30 are pending.

Claims 10, 11, 21, 23, and 28-30 were objected to for various informalities.

Claims 1, 6-13, and 20-22 were rejected under 35 U.S.C. § 102(a) for allegedly being anticipated by Pulkin et al, U.S. Patent No. 6,573,694.

Claims 2, 15, and 16 were rejected under 35 U.S.C. § 103(a) for being unpatentable over Pulkin et al., and Hsiao et al., U.S. Patent No. 3,984,780.

Claims 3-5, 14, and 17-19 were rejected under 35 U.S.C. § 103(a) for allegedly being unpatentable over Pulkin et al., Hsiao et al., and Miranda et al., U.S. 5,631,598.

Claims 23, 28, and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pulkin et al. and Xi, U.S. Patent No. 6,246,221.

Claims 24-27 and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pulkin et al., Xi, and Miranda et al.

Claims 10, 21, 23, and 28-30 have been amended accordingly to address the claim objections. A review of claim 11 does not reveal any objectionable informality. The claim objections are believed to be overcome.

The present invention is directed generally to a voltage regulator circuit. Figs. 1 and 6 are typical illustrative embodiments of the present invention as recited in the claims. An error signal produced by an amplifier component drives a source follower circuit via a series-connected resistor and transistor circuit. This causes the series-connected pair to produce a bias voltage, which is applied to the source follower. In a particular embodiment, the transistor is a component in a current mirror circuit.

The reference to Pulkin et al. does not show a source follower being driven by a series-connected resistor and transistor pair. Kindly refer to Fig. 2 of Pulkin et al., where they describe a buffer 30 comprising a source follower 34. There is no series-connected resistor and transistor pair.

The Hsiao et al. reference was cited for allegedly showing a source follower circuit driven by a current mirror. However, a review of Hsiao et al. does not appear to show

such a combination. Figs. 1 and 2 show a source follower configuration in transistor 4; however, there is no current mirror circuit. Figs. 3-5 show current mirror circuits; however, the current mirrors do not drive source follower circuits. For example, consider Fig. 3a. Transistor 4 is not configured as a source follower; its source terminal is at ground potential and so can not vary with the gate voltage. Moreover, the current mirror circuit comprising transistors 50 and 52 are not shown to be connect to transistor 4, in the first place. In Fig. 4a (see also Fig. 5a), the transistor 54 is not connected as a source follower; the source terminal is coupled to V_{DD} and so the potential at the source terminal will not vary with the gate voltage.

Miranda et al. was cited for showing a resistor configuration R3, R4 (Fig. 1) connected between a voltage rail and a transistor. It was asserted that doing so served to restrict current to the transistor and divide the source voltage. It was further asserted that this serves as the basis for modifying the Pulkin et al. circuit to provide a resistor to their source follower input. Respectfully, however, the general notion of restricting current and dividing source voltage is not a proper basis for making the proposed modification. There must be a teaching in the reference that suggests some reason for the proposed modification. The mere fact that a resistor serves to limit current cannot be a sufficient basis; all resistors limit current flow, that is a basic characteristic of resistors. The mere fact that the series combination of resistors R3 and R4 provides voltage division also cannot be a basis for the proposed modification. First, Miranda et al. do not quite show a voltage divider configuration in resistors R3 and R4. A proper voltage divider circuit would require R4 to be connected to ground. Second, even if R3 and R4 constitute a voltage divider, that fact in and of itself does not suggest its incorporation to the source follower of Pulkin et al. The teachings do not suggest making such a modification.

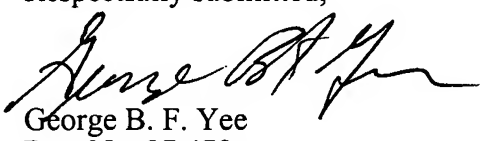
None of the foregoing references considered individually or in combination teach or suggest the combination of elements as recited in the pending claims. For example, the references do not show or suggest a series-connected resistor and transistor pair connected to a source follower. For at least this reason, the claim rejections are believed to be overcome.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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